The goal of the assignment is to develop a Moore Machine Sequence Detector which looks for the sequence **1101**, taking an input sequence ***a*** and having ***w*** as the output.

Start by designing the State Diagram for the 1101 Detector:

**STATE DIAGRAM – 1101 SEQUENCE DETECTOR**

**1**

**1**

**0**

**0**

**0**

**0**

Utilizing this diagram as a basis, develop the Stable Table of the 1101 Detector:

**STATE TABLE OF THE 1101 SEQUENCE DETECTOR**



Now create the state assignment matrix:

**STATE ASSIGNMENT TABLE**



With the state assignments, create the Transition Table for the 1101 Detector:

**TRANSITION TABLE FOR THE 1101 DETECTOR**



Using this Transition Table, derive the Flip-Flop Excitation Table:

**FLIP-FLOP EXCITATION TABLE**



With the Flip-Flop Excitation Table, develop the Karnaugh Maps for each of the flip-flops and the output. Then, use the Karnaugh Maps to determine logic needed to model the flip-flops and outputs in terms of the state variables:

**FLIP-FLOP KARNAUGH MAPS**



**D2 = x y1 y0**



**D1 = x y1 y0 + y1 y0 + x y2**



**D0 = x y2 y1 y0 + x y1 y0**



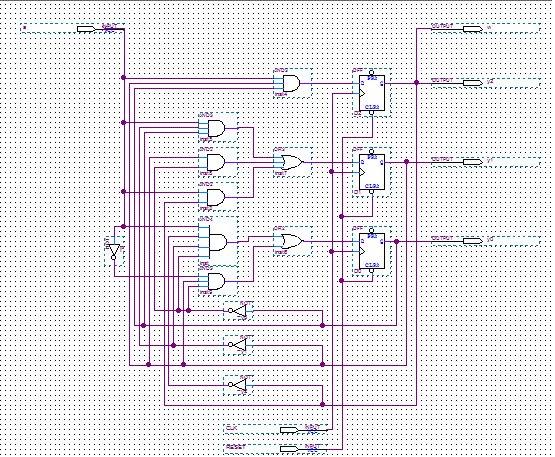
**w = y2**

Utilizing the equations from above, the following circuit can be constructed (done in MS Visio):



Here is a screenshot of the Quartus II circuit implementation:

**Quartus II Implementation of a 1101 Sequence Detector**



**A**

**Y0**

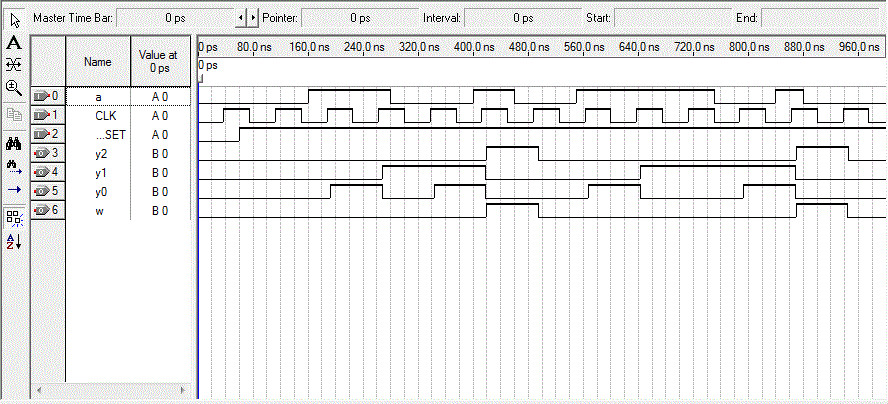
**Y2**

**Y1**

**W**

Below is the snapshot of the Quartus II waveform I used to test the implementation of the circuit, along with the simulation report confirming functionality:

**Waveform Simulation Report**



The two critical scenarios of the state-space representation were tested using this waveform, namely:

**GREEN SECTION:**

In this section, the input ***a*** is set to the sequence **1101** at four consecutive rising clock edges. It can be seen in the graph above that the output, ***w***, correctly becomes **1** once the sequence **1101** is seen.

**BLUE SECTION:**

In this section, the input ***a*** is set to the sequence **11101** at five consecutive rising clock edges. This scenario was chosen to prove that even after receiving consecutive **1**’s, the state-space representation could still find the sequence in question. It can be seen in the graph above that the output, ***w***, correctly becomes **1** once the sequence **1101** is seen (3 consecutive **1**’s, followed by **0 1**).